[0141] In addition, implanting fluorine ions can be performed to achieve a peak fluorine concentration located in the buffer layer **104** adjacent to the heterojunction or interface (e.g., under the 2DEG channel **1902**). In one non-limiting methodology, fluorine-19 ions can be implanted with a selected energy (e.g., 50 keV) at a selected dose (e.g., 1×10^{12} cm^{-2}) using an ion implanter (e.g., a Varian CF3000). In a further non-limiting methodology, fluorine ions can be implanted into the buffer layer **104** to form the back barrier region **206** under the design location of the HEMT gate **210** and reaching to a region under the design location of the HEMT source **208**.

[0142] In addition, methodologies **4500** can include steps preparatory to, or for completing, the HEMT device fabrication process, **4508**. As an example, steps preparatory to HEMT fabrication can include processes to facilitate isolation between different devices for example, by mesa etching (e.g., by inductively coupled plasma reactive ion etching), ion implantation, etc. For example, in the disclosed AlGaN/GaN EBB/LDD HEMTs, a low density drain **3702** structure can be formed, as described above, if not formed prior to this point in the fabrication process (e.g., prior to back barrier region **206** formation). For instance, a region of fluorine **3702** can be formed adjacent to the design location of the HEMT gate **210** and between the design location of the HEMT gate **210** and the design location of the HEMT drain **212**.

[0143] As another example, fluorine ions can be used to fabricate an enhancement-mode AlGaN/GaN HEMT **4100**, which can be achieved by incorporation of negatively charged fluorine ions into the AlGaN layer **106** under the gate **210** region **4102**. For instance, fluorine ions in the AlGaN layer **106** under the gate region **4102** can either be implanted by fluorine plasma treatment or low energy ion implantation, or using another suitable alternative. In addition, steps necessary to create a lateral field effect transistor can be performed as described above.

[0144] As a further example, additional resist strip, etch, clean, or other process steps (not shown) may be desired or required post-implant, depending on the design of the HEMT fabrication process. Also, additional process steps (not shown) may be employed to complete fabrication of the source **208**, gate **210**, drain **212**, etc. in order to complete fabrication of a useable device (e.g., either in isolation, or as part of an integrated circuit).

[0145] For example, a typical process of fabricating a Group III-nitride heterostructure field-effect transistor (HFET) comprises an epitaxial structure (e.g., substrate **102**, buffer layer **104**, and a barrier layer **106**), where the buffer layer **104** can be grown over a substrate, facilitated by a nucleation layer (e.g., low temperature grown GaN nucleation layer, AlGaN or AlN, etc.). A mesa isolation can be formed using a Cl_2/He plasma dry etching followed by source/drain ohmic contact formation with Ti/Al/Ni/Au annealed at 850 degrees Celsius for 30 seconds. Subsequently, photoresist can be patterned with the gate windows exposed. The gate electrode can be formed on the barrier layer by depositing and lift-off Ni and Au (e.g., with or without a dielectric insulator under the gate metal, or other variations, etc.). Thereafter, post-gate rapid thermal annealing (RTA) can be conducted at 400 to 450 degrees Celsius for 10 minutes. A passivation layer (e.g., SiN, silicon oxide(SiO), polyimide, Benzocyclobutene (BCB), etc.) can then be grown on top of the device. Finally, the contact pads can be opened by removing portions of the passivation layer on the contact pads.

[0146] Further non-limiting embodiments of methodologies **4500** (not shown) can include process steps to create a AlGaN/GaN V-HFET comprised of a substrate **4302**, upon which heavily doped GaN (N^+-GaN) **4304**, GaN (N^--GaN) **4306**, and an i-GaN/AlGaN (**1608**/**1610**) heterojunction is formed creating the 2DEG **4312** channel. As an example, fluorine ions can be implanted to create the fluorine implanted blocking region or layers **4314**, which can serve to improve source **4316** to drain **4318** isolation in the off-state of the AlGaN/GaN V-HFET **4300**, as more fully described above.

[0147] While the disclosed subject matter has been described in connection with the preferred embodiments of the various figures, it is to be understood that other similar embodiments may be used or modifications and additions may be made to the described embodiments for performing the same function of the disclosed subject matter without deviating therefrom. For example, one skilled in the art will recognize that aspects of the disclosed subject matter as described in the various embodiments of the present application may apply to other Group III-Nitride heterostructures, other insulating or semiconducting materials or substrates, etc.

[0148] As a further example, in addition to the disclosed buffer layer **104** and barrier layer **106**, it is conceivable that other layers for purposes other than described in one or more embodiments herein can be introduced between the buffer layer **104** and barrier layer **106**. However, in such cases, such intermediate layers, without effect, can be considered as part of the buffer layer **104** or part of the barrier layer **106**. Moreover, sometimes layers inadvertently introduced (e.g., process contaminants, oxidation, natural impurities, etc.) are also formed as a byproduct of an industrial fabrication process and such layers also are not to be considered separate layers.

[0149] In other instances, variations of process parameters (e.g., dimensions, configuration, concentrations, concentration profiles, implant energies and doses, process step timing and order, addition and/or deletion of process steps, addition of preprocessing and/or post-processing steps, etc.) may be made to further optimize the provided structures, devices and methodologies, as shown and described herein. In any event, the structures and devices, as well as the associated methodologies described herein have many applications in high electron mobility transistor heterostructures. Therefore, the disclosed subject matter should not be limited to any single embodiment described herein, but rather should be construed in breadth and scope in accordance with the appended claims.

What is claimed is:

1. An aluminum gallium nitride/gallium nitride (AlGaN/GaN) high electron mobility transistor (HEMT), the HEMT having prospective locations for a source, a gate, and a drain, the HEMT comprising:

a substrate;

a buffer layer comprising gallium nitride (GaN) disposed on the substrate;

a barrier layer comprising aluminum gallium nitride (AlGaN) disposed on the buffer layer and forming a heterojunction at an interface of the barrier layer and the buffer layer; and

an enhanced back barrier (EBB) region of implanted fluorine disposed within the buffer layer and spanning a portion of the heterojunction.

2. The AlGaN/GaN HEMT of claim **1**, the substrate comprising at least one of sapphire, silicon (111), silicon carbide (SiC), aluminum nitride (AlN), or GaN.